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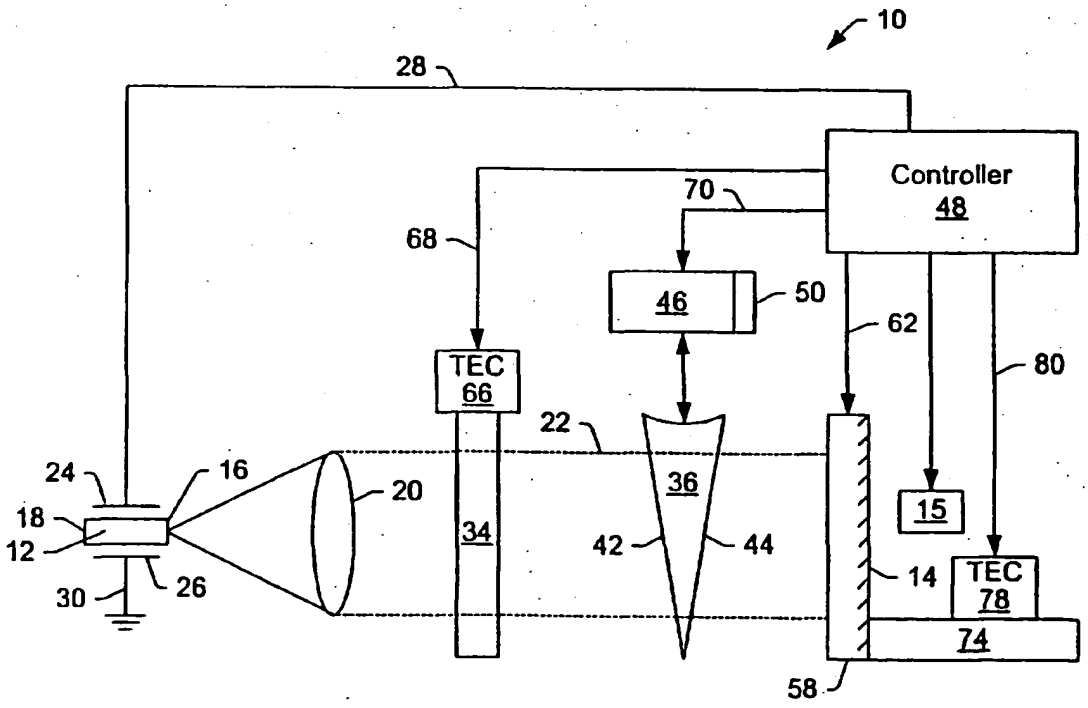
(54) Title: TUNABLE LASER CONTROL SYSTEM



(57) Abstract: A laser system including a controller for monitoring and controlling various functions of a laser assembly. The laser controller may include a wavelength tuning circuit for adjusting and locking the wavelength of the external cavity. To perform various monitoring and control functions, the controller may include circuitry for monitoring various parameters associated with operation of the laser, such as temperature indicating signals and/or signals from light detectors such as photodiodes.

WO 03/005512 A2

TITLE: TUNABLE LASER CONTROL SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to laser systems and, more particularly, to electronic controllers for controlling and monitoring operations of a tunable laser, such as an external cavity diode laser.

2. Description of the Related Art

Tunable external cavity diode lasers (ECDLs) are widely used in lightwave test-and-measurement equipment and are becoming recognized as essential components for the rapidly expanding fields of wavelength division multiplexed (WDM) optical voice and data communications. The many applications within these fields represent many different sets of performance specifications. However, the following requirements are typical: small size of the optomechanical assembly and control system; servo control of the wavelength; and controllable frequency modulation (FM) at audio rates (e.g., 100 Hz to 30 kHz) in order to broaden the linewidth.

To achieve desired control over the operation of external cavity diode lasers, electronic controllers are typically provided that implement various functionality. This functionality may include a current source for providing current to the laser, locked wavelength tuning functionality, a modulation source, and various oth r functionality to precisely control and monitor operation of the tunable laser. It is typically desirable that the electronic controller allow for versatile control of the tunable laser with reasonable efficiency and a relatively small form factor. It is also typically desirable that electrical noise within the system and its impact upon various measurement functions be minimized.

SUMMARY OF THE INVENTION

A laser control system for monitoring and controlling various functions of a laser assembly is provided. In one embodiment, the laser assembly comprises a tunable external cavity laser. The laser controller may include a wavelength tuning circuit for adjusting and locking the wavelength of the external cavity. The tuning circuit may include a modulation signal generator for providing a modulation signal to a selected transmission element that causes a corresponding modulation of the optical path of the laser external cavity. Wavelength locking may be achieved by monitoring transmission characteristics that vary due to the slight modulation of the optical path. Such transmission characteristics may be monitored, for example, by detecting variations in the voltage across a gain medium or variations in the intensity of light associated with the laser external cavity. The tuning circuit may include a signal processor such as a microprocessor that performs a Fourier Transform, such as a Fast Fourier Transform, upon data indicative of the transmission characteristics to thereby generate an error signal for adjusting the length of the optical path of the external cavity.

To perform various monitoring and control functions, the controller may include circuitry for monitoring various parameters associated with operation of the laser, such as temperature indicating signals and/or signals from light detectors such as photodiodes. The controller may additionally detect other parameters, such as a voltage across a gain medium. In one embodiment, the sensing of such parameters is performed synchronously with the generation of various control signals for controlling operation of the external cavity laser. The control signals may

Gain medium 12 emits a coherent beam from rear facet 16 that is collimated by lens 20 to define an optical path 22 which is co-linear with the optical axis of the external cavity. Rear and front facets 16, 18 of gain medium 12 are aligned with the optical axis of the external cavity as well. Light reflected from end mirror 14 is fed back along optical path 22 into gain medium 12. Conventional output coupler optics (not shown) may be associated with front facet 18 for coupling the output of external cavity laser 10 into an optical fiber (also not shown).

Transmission characteristics of the external cavity can be probed or evaluated by monitoring the voltage across gain medium 12. In this regard, first and second electrodes 24, 26 may be positioned adjacent to and operatively coupled to gain medium 12. First electrode 24 is operatively coupled to a controller 48 via a conductor 28, where the voltage across gain medium 12 may be detected. A second electrode 26 is grounded via conductor 30. It is noted that in various other embodiments, transmission characteristics of the external cavity may be alternatively evaluated by monitoring the output of one or more photodiodes 15 (or any other type of light detector) that may be positioned to receive portions of light associated with the external cavity laser. For example, in one embodiment, a photodiode may be positioned to detect light propagating through the partially reflective end mirror 14. In another embodiment, a photodiode may be positioned to detect light propagating through front facet 18 of gain medium 12. Photodiodes may be positioned to detect light associated with the external cavity laser at other particular locations, as desired.

Error signals may be derived from the voltage measured across gain medium 12 to correct or otherwise adjust the transmission characteristics associated with the external cavity. Details regarding specific implementations of this functionality are provided further below.

Other transmission elements associated with the external cavity may include a grid generator element and a channel selector element, which are respectively shown in FIG. 1 as a grid etalon 34 and a wedge etalon 36 positioned in optical path 22 between gain medium 12 and end mirror 14. Grid etalon 34 typically is positioned in optical path 22 before wedge etalon 26. Grid etalon 34 operates as an interference filter, and the refractive index and optical thickness of grid etalon 34 give rise to a multiplicity of minima within the communication band at wavelengths which coincide with the center wavelengths of a selected wavelength grid which may compris , for example, the ITU (International Telecommunications Union) grid. Other wavelength grids may alternatively be selected. Grid etalon 34 thus has a free spectral range (FSR) which corresponds to the spacing between the grid lines of the ITU grid or other selected grid, and the grid etalon 34 thus operates to provide a plurality of pass bands centered on each of the gridlines of the wavelength grid. Grid etalon 34 has a finesse (free spectral range divided by full width half maximum or FWHM) which suppresses neighboring modes of the external cavity laser between each channel of the wavelength grid.

Grid etalon 34 may be a parallel plate solid, liquid or gas spaced etalon, and may be tuned by precise dimensioning of the optical thickness between its faces by thermal expansion and contraction via temperature control. The grid etalon 34 may alternatively be tuned by tilting to vary the optical thickness between faces 38, 40, or by application of an electric field to an electro-optic etalon material. Various other grid generating elements are known to those skilled in the art and may be used place of grid etalon 34. Grid etalon 34 may be thermally controlled using a temperature controller (TEC) 66 to prevent variation in the selected grid which may arise due to thermal fluctuation during operation of external cavity laser 10. Grid etalon 34 alternatively may be actively tuned during laser operation.

translates or drives wedge etalon 36 to a position wherein the optical thickness of the portion of the wedge etalon 36 positioned in optical path 22 provides constructive interference which supports the selected channel. A position detector 50 such as a linear encoder may be used in association with wedge etalon 36 and drive element 46 to ensure correct positioning of wedge etalon 36 by driver 46. Alternatively, a single point position electro-optic detector may be provided to locate a "home" position associated with wedge etalon 36 during initialization of the system.

An electro-optically activated modulation element 58 is also shown positioned in optical path 22 before end mirror 14. In the embodiment of FIG 1, end mirror 14 is formed as a reflective coating directly on the electro-optic material of modulation element 58. Thus, the end mirror 14 and modulation element 58 are combined into a single component. In other embodiments, end mirror 14 may be formed on an element that is separate from modulation element 58. Details regarding the function of modulation element 58 will be provided further below.

The pass band relationship of the grid etalon 34, wedge etalon 36 and the external cavity defined by front facet 18 and end mirror 14 are illustrated graphically in FIG. 2A through FIG. 2C, which show external cavity pass bands PB1, grid etalon pass bands PB2, and wedge etalon pass bands PB3. Relative gain is shown on the vertical axis and wavelength on the horizontal axis. As can be seen, free spectral range of the wedge etalon 36 ($FSR_{Channel\ Sel}$) is greater than the free spectral range of the grid etalon 34 ($FSR_{Grid\ Gen}$), which in turn is greater than the free spectral range of the external cavity (FSR_{Cavity}). The band pass peaks PB1 of the external cavity periodically align with the center wavelengths of pass bands PB2 defined by the wavelength grid of grid etalon 34. There is one pass band peak PB3 from the wedge etalon 36 which extends over all of the pass bands PB2 of the wavelength grid. In the specific example shown in FIG. 2A-2C, the wavelength grid extends over sixty four channels spaced apart by one half nanometer (nm) or 62GHz, with the shortest wavelength channel at 1532 nm, and the longest wavelength channel at 1563.5 nm.

The finesse of grid etalon 34 and wedge etalon 36 determine the attenuation of neighboring modes or channels. As noted above, finesse is equal to the free spectral range over the full width half maximum, or finesse = FSR/FWHM. The width for a grid etalon pass band PB2 at half maximum is shown in FIG. 2B, and the width for a wedge etalon pass band PB3 at half maximum is shown in FIG. 2C. The positioning of grid etalon 34 and wedge etalon 36 within the external cavity improves side mode suppression.

The tuning of the band pass PB3 of wedge etalon 36 between a channel centered at 1549.5 nm and an adjacent channel at 1550 nm is illustrated graphically in FIG. 3A-3C, wherein the selection of a channel generated by grid etalon 24 and the attenuation of adjacent channels or modes is shown. The external cavity pass bands PB1 shown in FIG. 2A-2C are omitted from FIG. 3A-3C for clarity. The grid etalon 34 selects periodic longitudinal modes of the external cavity corresponding to the grid channel spacing while rejecting neighboring modes. The wedge etalon 36 selects a particular channel in the wavelength grid and rejects all other channels. The selected channel or lasing mode is stationary at one particular channel for filter offsets in the range of approximately plus or minus one half channel spacing. For larger channel offsets the lasing mode jumps to the next adjacent channel.

In FIG. 3A, the wedge etalon pass band PB3 is centered with respect to the grid channel at 1549.5 nm. The relative gain associated with pass band PB2 at 1549.5 nm is high, while the relative gain levels associated with adjacent pass bands PB2 at 1549.0 nm and 1550.0 nm are suppressed relative to the selected 1549.5 nm channel. The gain associated with pass bands PB2 at 1550.5 nm and 1548.5 nm is further suppressed. The dashed line indicates the relative gain for pass bands PB2 without suppression by wedge etalon 36.

A tuning arm 74 may further be employed to positionally adjust end mirror according to input from controller 48. Tuning arm 74 may be made from a material having a high coefficient of thermal expansion, such as aluminum or other metal or metal alloy. Controller 48 is operatively coupled to a thermoelectric controller 78 via line 80. Thermoelectric controller 78 is coupled to tuning arm and is configured to adjust the temperature of arm 74. Thermal control (heating or cooling) of tuning arm 74, according to signals from controller 76, may be used in this embodiment to control the position of end mirror 14 and the length of optical path *l* of the external cavity defined by end mirror and front facet 18 of gain medium 12 in an optimal position.

The frequency modulation introduced by modulation element 58 is detectable by controller 48 by monitoring the voltage across the gain medium 12 or a signal from one or more photodiodes 15, and the frequency modulation includes variations in magnitude and phase error indicative of laser cavity mode alignment with the center wavelength of the pass bands defined by grid generator 34 and channel selector 36, as noted above. Controller 48 may be configured to derive an error signal from the modulation introduced by the frequency dither, and to communicate a compensation signal to thermoelectric controller 78, which accordingly heats or cools tuning arm 74 to position end mirror 14 and adjust the optical path length *l* of external cavity laser to null out the error signal.

FIG. 4 is a functional block diagram illustrating aspects of one embodiment of controller 48. The controller of FIG. 4 includes a tuning circuit 84, a current source 86 operatively coupled to gain medium 12 via line 28, a grid controller 88 operatively coupled to thermoelectric controller 66 via line 68, and a channel controller 90 operatively coupled to drive element 46 via line 70. The current source 86 controls the power delivered to gain medium 12. The grid controller 88 maintains the referential integrity of grid etalon 34 by thermal control thereof using thermoelectric controller 66 to heat or cool grid etalon 34 as required. Channel controller 90 directs drive element 46 to position or otherwise adjust channel selector 36 for selection of desired transmission bands in the grid defined by grid etalon 34.

Tuning circuit 84 comprises a signal processor 94, a voltage detector 96, a path length adjuster 100, and a modulation signal generator 102. Modulation signal generator 102 provides a frequency dither or modulation signal to a selected loss element (e.g., modulation element 58) that causes a corresponding modulation of the optical path *l* of the laser external cavity. The modulation frequency and amplitude may be selected, for example, to increase effective coupling efficiency. The voltage across gain medium 12 (or a signal derived from a photodiode 15, as discussed previously) may be detected by voltage detector 96 and communicated to signal processing circuit 94. The signal processing circuit 94 may be configured to determine the alignment of passbands PB1 (FIG. 2 and FIG. 3) of the external cavity with passbands PB2 of grid etalon 34 and passbands PB3 of channel selector 36, and to generate corresponding error information.

Pathlength adjuster 100 generates an error correction or compensation signal, from the error information provided by signal processing 94, that is used to adjust the optical path length *l* of the external cavity in order to optimize the relationship between the modulation signal and the intensity signal. When an external cavity mode or pass band PB1 is aligned with bands PB2 and PB3 generated by grid generator 34 and channel selector 36, intensity variations at the modulation frequency (and odd multiples thereof) in the coherent beam traveling optical path 22 are substantially minimized, as discussed further below with reference to FIG. 5. Concurrently, the voltage signal intensity will vary at twice the modulation frequency. Either or both of these detectable effects are usable to evaluate external cavity loss associated with loss characteristics associated with the positioning or inter-relationship

FIG. 6 is a hardware block diagram illustrating various aspects of one embodiment of a laser controller that may be configured to implement the functionality of the control system as depicted in FIG. 4. Various features of a laser assembly such as the assembly 10 described previously in conjunction with FIG. 1 are also illustrated in FIG. 6. Features that correspond to those of FIG. 1 and FIG. 4 are numbered identically for simplicity and clarity. It is noted that in other embodiments, various features of the laser controller of FIG. 6 as discussed below may be used in conjunction with other configurations of laser assemblies. Furthermore, such controllers and laser assemblies may omit various functionality as discussed above in conjunction with FIGS. 1 – 5.

The laser controller of FIG. 6 includes a microprocessor (CPU) 602 coupled through an interconnect bus 610 to a read-only memory (ROM) 604, a random access memory (RAM) 606 and a field programmable gate array (FPGA) 608. FPGA 608 is coupled to a stepper motor driver 612, amplifiers 614-616, and a low pass filter 618. FPGA 608 is further shown coupled to a digital-to-analog converter 620, an analog interface unit 622, and an analog-to-digital converter 624. A laser current source 86 is shown coupled to an output of digital-to-analog converter 620.

Power to the components of the laser controller illustrated in FIG. 6 is provided by a power source 630. In one embodiment, power source 630 receives 5 volt input power and generates output power of varying voltage levels to appropriately supply power to the components of controller 600. Power source 630 may be implemented using a high efficiency switching regulator circuit.

Microprocessor 602 and FPGA 608 operate concurrently and in cooperation with each other to perform various functionality as depicted in FIG. 4 and described hereinbelow. It is noted that operations performed by microprocessor 602 may be conducted in accordance with the execution of software code stored within ROM 604. In one embodiment, microprocessor 602 is implemented using a general purpose microprocessor, such as a Motorola MCF5206e microprocessor. It is noted that in other embodiments, a digital signal processor or other specialized hardware may be employed in place of microprocessor 602. It is further noted that in other embodiments, other programmable logic devices, such as a CPLD (Complex Programmable Logic Device) may be employed in the place of FPGA 608. Alternatively, one or more ASICs (Application Specific Integrated Circuits) could be employed. Still additional embodiments are contemplated that combine various functionality of microprocessor 602 and FPGA 608 as described herein within a single device.

Generally speaking, microprocessor 602 and FPGA 608 collectively operate to measure and process various parameters associated with the operation of laser assembly 10 and to perform various control functions. In one particular implementation, microprocessor 602 and FPGA 608 are clocked at 40 MHz.

As illustrated in FIG. 6, laser assembly 10 may include a laser temperature sensor 631 located in proximity to gain medium 12, a grid generator temperature sensor 632 located in proximity to grid etalon 34, a cavity length actuator temperature sensor 633 located in proximity to tuning arm 74, and an ambient temperature sensor 634. Each of the sensors 631-634 may be implemented using a thermistor, although other temperature dependent devices may be employed in other embodiments. Laser assembly 10 may further include one or more photodiodes 15 positioned at selected locations of the laser assembly to receive light associated with the operation of the external cavity laser. In the illustrated embodiment, FPGA 608 may be programmed to periodically detect signals associated with each of sensors 631-634, photodiodes 15, and/or gain medium 12 through analog interface 622 and analog-to-digital converter 624. For this purpose, analog interface 622 includes multiplexers 650-652 and an anti-alias filter 653. Multiplexers 650-652 operate under the control of FPGA 608 to periodically couple a signal associated with a

In one particular implementation, following a predetermined settling time after FPGA 608 sets multiplexers 650 and 652 in a manner to convey a signal corresponding to the voltage across gain medium 12 to analog-to-digital converter 624, FPGA 608 performs a burst of, for example, 50 separate and consecutive voltage readings associated with the voltage across gain medium 12. Each of the voltage readings (in the form of digital data generated by analog-to-digital converter 624) may be temporarily stored within FPGA 608, and is subsequently transferred into RAM 606. Upon receipt of data from analog-to-digital converter 624 by FPGA 608, FPGA 608 may signal microprocessor 602 which may responsively invoke an internal direct memory access control mechanism to carry out the transfer of the data from FPGA 608 to RAM 606.

Upon storing a set of data indicative of the voltage across gain medium 12 within RAM 606, microprocessor 602 performs a Fourier Transform to transform the temporal data to a frequency domain to separate the DC, fundamental and/or harmonic terms. In one embodiment, microprocessor 602 executes a Fast Fourier Transform (FFT) routine. The FFT routine may be optimized for integer input data as supplied from analog-to-digital converter 624, and may be configured to compute only the output terms of particular interest, such as the fundamental component. As discussed previously, by calculating, for example, the magnitude and phase of the fundamental component, an error signal may be generated to adjust the cavity length. Thus, upon calculation of the error signal, microprocessor 602 writes a value derived from the error signal to a location within FPGA 608 which controls the pulse width of the PWM signal provided to amplifier 616 to drive cavity length actuator temperature controller 78. It is noted that in other embodiments, the error signal may be used to control other mechanisms within a laser assembly to adjust cavity length. It is also noted that in other embodiments, similar measurements may alternatively be taken from one or more photodiodes 15 (or other light detectors) to derive the error signal. In various embodiments and depending upon the signals of interest, multiplexer 650 and/or anti-alias filter 653 of analog interface 622 may be omitted.

FIG. 6A illustrates one embodiment of an algorithm for performing wavelength-locking. The wavelength-locking algorithm as depicted in FIG. 6A may be implemented by code executed within microprocessor 602, and in conjunction with the control of FPGA 608 as described herein. When initiated, the algorithm begins by computing offsets, initializing variables, and placing the cavity length actuator 78 in an initial starting position (steps 670 and 671). Next, the algorithm enters a locking loop where the cavity length actuator sensor 633 is measured and the quality of the locking is determined. The quality of locking may be determined by computing a decaying integral of the error signal. If the cavity length actuator sensor indicates a temperature within a predetermined range and if the lock quality is sufficient as determined during step 672, modulation data is acquired during step 673. As discussed previously, the modulation data may be in the form of a set of readings associated with the voltage across gain medium 12, or may be associated with a set of readings taken from one or more photodiodes 15. The fundamental modulation component of the most recent gain medium potential measurement may be used to compute cavity length errors (step 674) and is applied to a compensator in order to minimize the fundamental component. As stated previously, the fundamental modulation component may be computed by an FFT routine executed by microprocessor 602. In other embodiments, other harmonics of the gain medium voltage or photodiode currents may alternatively or additionally be determined and used to compute the error signal. The slew rate associated with the error signal may be limited during step 675. During step 676, microprocessor 602 may write a value in a corresponding storage location of FPGA 608 that controls the generation of the PWM signal to cavity length actuator temperature controller 78 to thereby cause corrections to the cavity length to be made. The locking

resistor 717 and capacitor 719 may provide residual noise attenuation at mid and upper frequencies. Current flowing through transistor 702 is sensed in accordance with sense resistor 704 and an operational amplifier 722. More particularly, operational amplifier 722 is configured to sense the current flowing through transistor 702 by measuring the voltage across resistor 704. The output of operational amplifier 722 is reflected down to a ground-based voltage using transistor 725, which regulates current flow through a resistor 723 depending upon the voltage across resistor 704. Thus, the voltage at node 721 is a ground referenced voltage indicative of the current flowing through transistor 702. It is noted that the circuit configuration of FIG. 7 allows one of the nodes (e.g., the cathode) of gain medium 12 to be grounded.

The current source of FIG. 7 further includes a transistor 708 connected in a common gate configuration between a node 710 and the gate of transistor 702. In the embodiment shown, transistor 708 is implemented using a FET (field effect transistor). In other embodiments, transistor 708 may be implemented using a bi-polar transistor coupled in a common base configuration. Due to the high output impedance looking into the drain of transistor 708, lower frequency noise on the power supply at node 712 is reflected onto the gate of transistor 702 thus causing V_{GS} to remain constant. Transistor 708 provides level translation up to the gate of transistor 702 without introducing a significant power supply voltage dependence. Thus, while the current flowing through transistor 702 will be dependent upon the voltage at node 710 which is controlled by the output of operational amplifier 716, the output current of transistor 702 is largely unaffected by low frequency noise on the power supply at node 712. Operational amplifier 716 maintains the DC current at the programmed level.

Switch 730, which may be implemented using a transistor such as a FET or bi-polar transistor, provides the user with a fast acting laser shutdown. Preferably, switch 730 may have a low voltage threshold so even in a worst-case, a relatively low voltage may be sufficient to drive the transistor into conduction and divert the current source from the gain medium 12. It is noted that control of the switch 730 may be conducted independent of the operation of microprocessor 602 (FIG. 5). Thus, the laser may be shut down even if malfunctions associated with the execution of instructions by microprocessor 602 occur.

It is noted that in other embodiments, other particular current source circuits may be employed for providing current to gain medium 12. Such alternative circuit configurations may employ a drive transistor for supplying current to a laser device, a control circuit for controlling the level of current supplied to the laser device, and a common gate transistor (or common base transistor) coupled between the control circuit and a control terminal of the drive transistor to reduce the effects of noise. Such circuits may additionally employ a switch for diverting current from the laser device.

FIG. 8 illustrates one embodiment of analog interface 622 for the measurement of temperatures within laser assembly 10. Circuit portions that correspond to those of FIG. 6 are numbered identically. FIG. 9 is a flow diagram depicting a method for temperature measurements.

Referring collectively to FIGS. 6, 8 and 9, FPGA 608 sets multiplexers 651 and 652 in modes to selectively convey a signal generated by one of the temperature sensors 631-634 or other input to analog-to-digital converter 624 for data capture within FPGA 608. Additional multiplexer 651 inputs include a ground reference 802 and a precision reference 804. Precision reference input 804 may be implemented using a precision resistor. Depending upon the mode of multiplexer 651 as controlled by FPGA 608, one input at a time is coupled to the output of multiplexer 651, which in turn is coupled to a fixed voltage reference through a fixed resistance 806. Thus, one of the temperature sensors 631-634 or precision reference 804 may be connected to form the lower leg of voltage

D amplifier may be coupled to drive the primary of transformer 1004 through an LC filter, and may be coupled in a push-pull configuration.

As a result of the push-pull configuration, a voltage of approximately $2V_{CC}$ peak-to-peak variations (twice the supply voltage) may be generated across the primary of transformer 1004. Return current through the primary of transformer 1004 is passed through operational amplifier 1008, rather than running return current through ground. Noise due to the generation of the 20 kHz modulation signal on the ground reference may thereby be reduced. In one embodiment, transformer 1004 has a coil ratio of 120 to 1, thereby generating a voltage of up to 1000 volts peak to peak at the output of the secondary of the transformer 1004 to drive the modulation element 58.

Although the embodiments above have been described in considerable detail, numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.

13. The method as recited in claim 12 wherein said control signal is a pulse-width modulated signal for controlling an external cavity length of said tunable laser.

14. The method as recited in claim 12 wherein said attribute is a voltage across a gain medium.

15. A controller for a tunable laser comprising:
means for generating a control signal to control the tunable laser; and
means for sensing an attribute associated with operation of the tunable laser synchronously with generation of said control signal.

16. The controller as recited in claim 15 wherein said control signal is a pulse-width modulated signal for controlling an external cavity length of said tunable laser.

17. The controller as recited in claim 15 wherein said attribute is a voltage across a gain medium.

18. A laser system comprising:
a tunable laser; and
a controller coupled to the tunable laser, the controller including:
a control circuit for generating a control signal to control the tunable laser; and
a sensing circuit for sensing an attribute associated with operation of the tunable laser;
wherein the sensing circuit senses said attribute synchronously with generation of said control signal by said control circuit.

19. The laser system as recited in claim 18 wherein the control signal controls an external cavity length of said tunable laser.

20. The laser system as recited in claim 18 wherein said control signal is a pulse width modulated signal.

21. The laser system as recited in claim 21 wherein said pulse width modulated signal controls an external cavity length of said tunable laser.

22. The laser system as recited in claim 21 wherein said pulse width modulated signal is provided to a temperature controller.

23. The laser system as recited in claim 18 wherein said tunable laser includes a gain medium, wherein said attribute sensed by said sensing circuit is a voltage across said gain medium.

24. A temperature sensing circuit comprising:
a plurality of temperature-dependent resistive elements;

33. The laser system as recited in claim 30 wherein one of said plurality of temperature-dependent resistive elements is placed in proximity to a grid generator for sensing a temperature associated with the grid generator.

34. The laser system as recited in claim 30 wherein one of said plurality of temperature-dependent resistive elements is placed in proximity to a cavity length actuator for sensing a temperature associated with the cavity length actuator.

35. A control circuit for generating a modulating output signal for driving an optical path length modulator in a tunable laser comprising:

waveform generation circuitry for generating an analog signal;

an amplifier circuit to receive the analog signal and configured to produce an amplified analog signal; and

a transformer including a primary coil coupled to the amplifier circuit in a push-pull configuration and a secondary coil for providing the modulating output signal.

36. The control circuit as recited in claim 35 wherein the waveform generation circuitry includes a programmable logic device for generating a digital output signal.

37. The control circuit as recited in claim 36 wherein a signal conversion circuit converts said digital signal to said analog signal.

38. The control circuit as recited in claim 37 wherein the signal conversion circuit comprises a low-pass filter.

39. The control circuit as recited in claim 38 wherein said digital signal is a pulse width modulated signal.

40. The control circuit as recited in claim 35 wherein said amplifier circuit includes a pair of operational amplifiers having outputs coupled to source and sink current flowing through said primary coil of said transformer.

41. A laser system comprising:

a tunable laser including an optical path length modulator; and

a control circuit for generating a modulating output signal for driving the optical path length modulator, the control circuit including:

waveform generation circuitry for generating an analog signal;

an amplifier circuit to receive the analog signal and configured to produce an amplified analog signal; and

a transformer including a primary coil coupled to the amplifier circuit in a push-pull configuration and a secondary coil for providing the modulating output signal.

42. The laser system as recited in claim 41 wherein the waveform generation circuitry includes a programmable logic device for generating a digital output signal.

a drive transistor having an output for supplying current to the laser gain medium device and a control terminal;

a control circuit for receiving a signal to control a level of current supplied to the laser gain medium device;

a power source;

a resistor coupled between the power source and the control terminal of the drive transistor; and

a common control terminal transistor, coupled between the control circuit and the control terminal of the drive transistor.

55. A laser control circuit for performing wavelength locking in a tunable laser comprising:

a pathlength adjuster circuit for controlling a pathlength associated with said tunable laser;

a modulation generator for providing a modulation of said pathlength;

a detector configured to detect an attribute of said tunable laser that is dependent upon said modulation and to generate data indicative of said attribute; and

a signal processing device configured to perform a Fourier Transform upon said data to derive an error signal for controlling said pathlength adjuster circuit.

56. The laser control circuit as recited in claim 55 wherein the signal processing device is configured to perform a Fast Fourier Transform.

57. A method for performing wavelength locking in a tunable laser comprising:

setting a pathlength associated with said tunable laser;

providing a modulation of said pathlength;

detecting an attribute of said tunable laser that is dependent upon said modulation;

generating data indicative of said attribute;

performing a Fourier Transform upon said data to derive an error signal; and

controlling said pathlength depending upon said error signal.

58. A laser control circuit for performing wavelength locking in a tunable laser comprising:

means for setting a pathlength associated with said tunable laser;

means for providing a modulation of said pathlength;

means for detecting an attribute of said tunable laser that is dependent upon said modulation;

means for generating data indicative of said attribute;

means for performing a Fourier Transform upon said data to derive an error signal; and

means for controlling said pathlength depending upon said error signal.

59. A laser system comprising:

a tunable laser assembly;

a control circuit for controlling operation of said tunable laser assembly; and

a network interface coupled to said control circuit and configured to allow remote control of said operation of said tunable laser through said network interface.

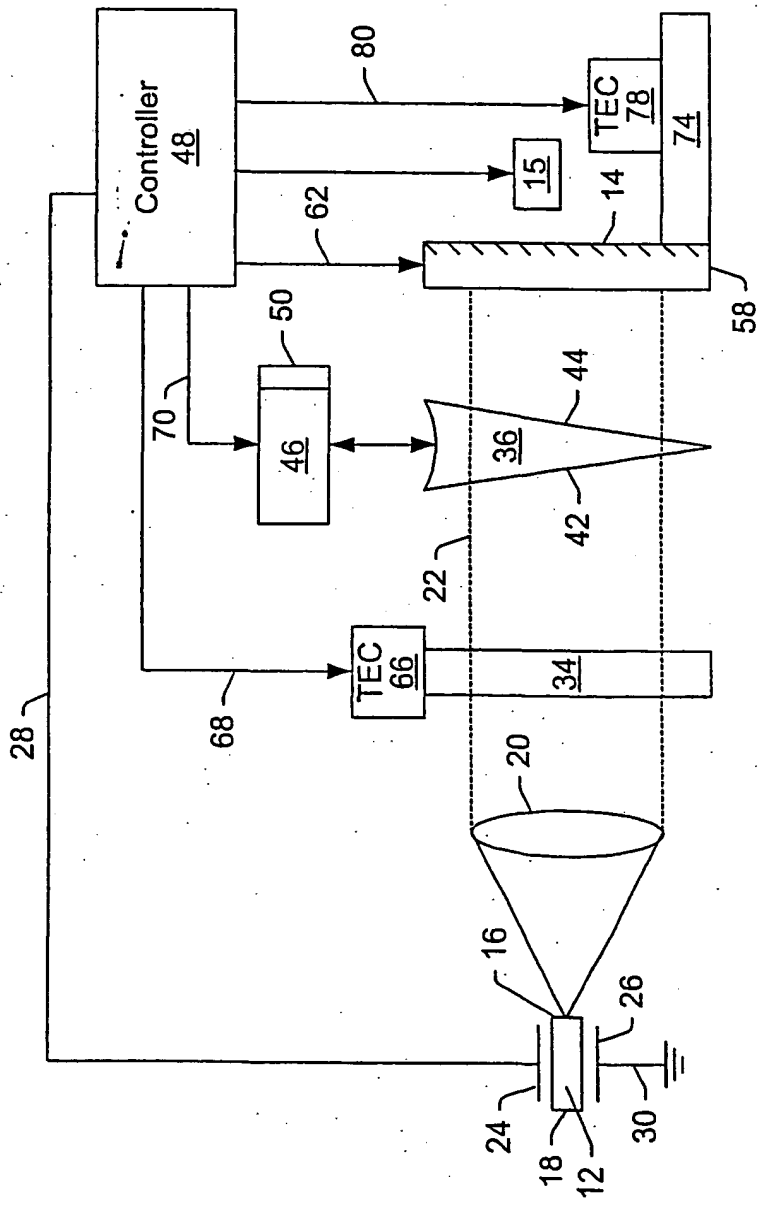

10
Controller
48
80
TEC
78
74
15
14
62
58
50
70
46
44
36
42
22
TEC
66
34
68
28
20
16
26
24
18
12
30

Fig. 1

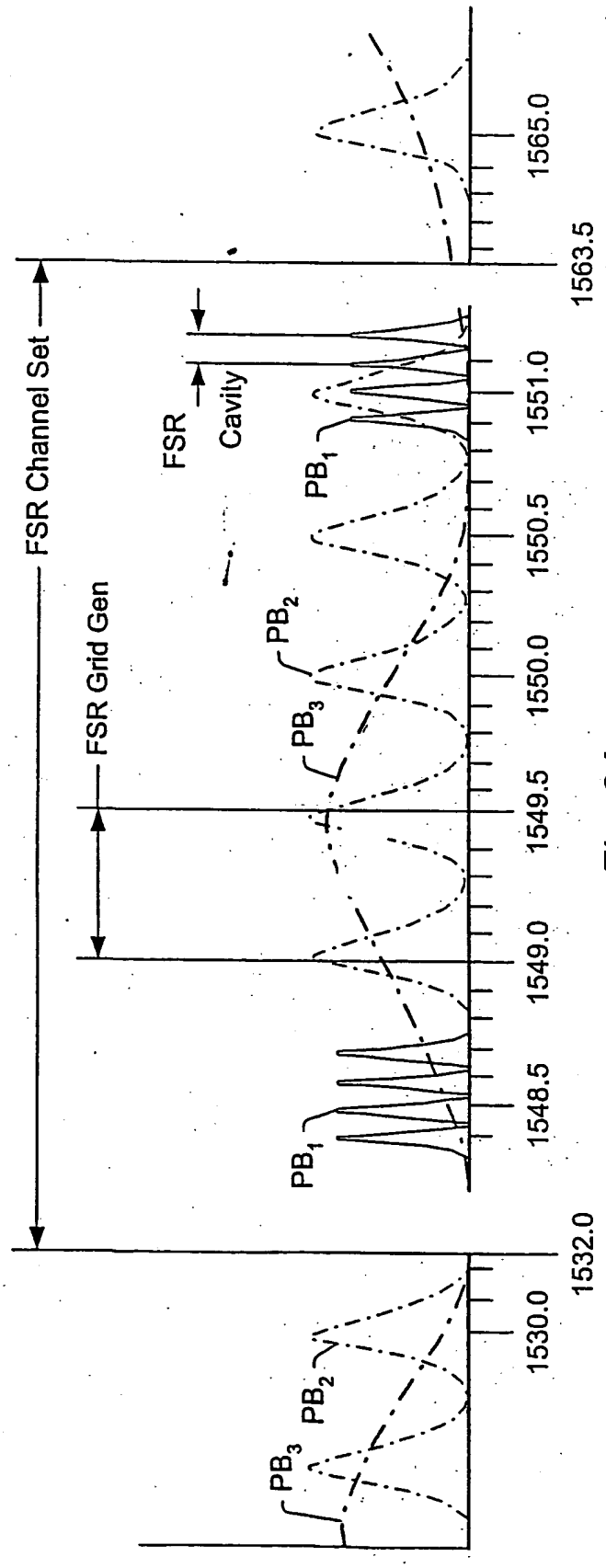


Fig. 2A

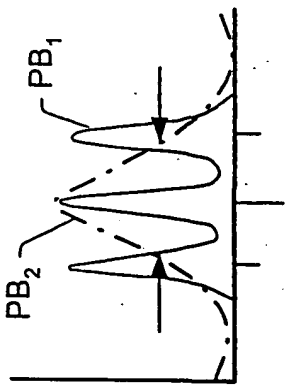


Fig. 2B

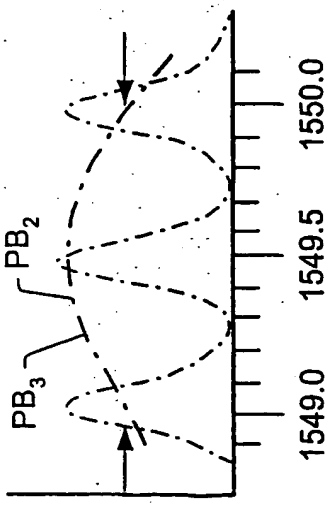


Fig. 2C

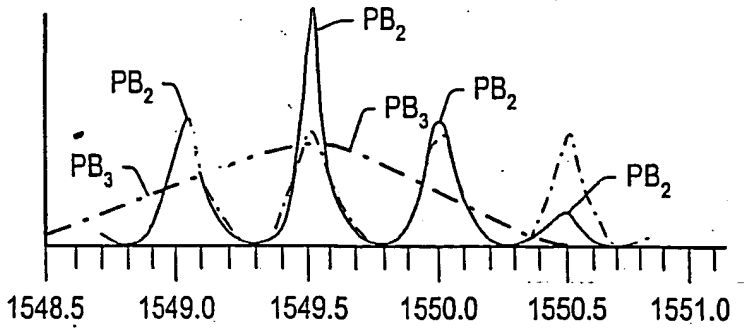


Fig. 3A

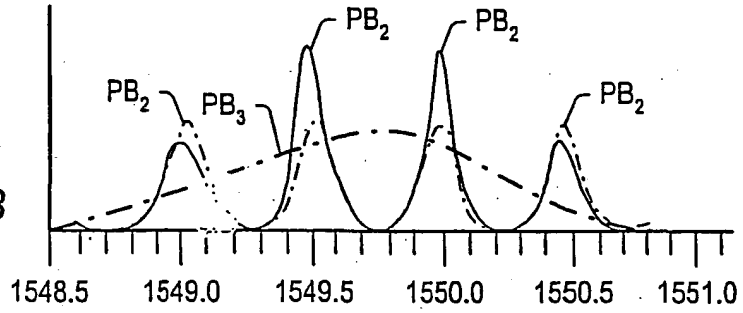


Fig. 3B

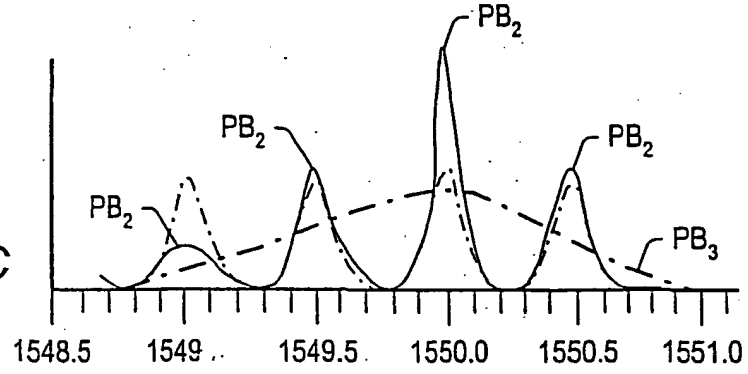


Fig. 3C

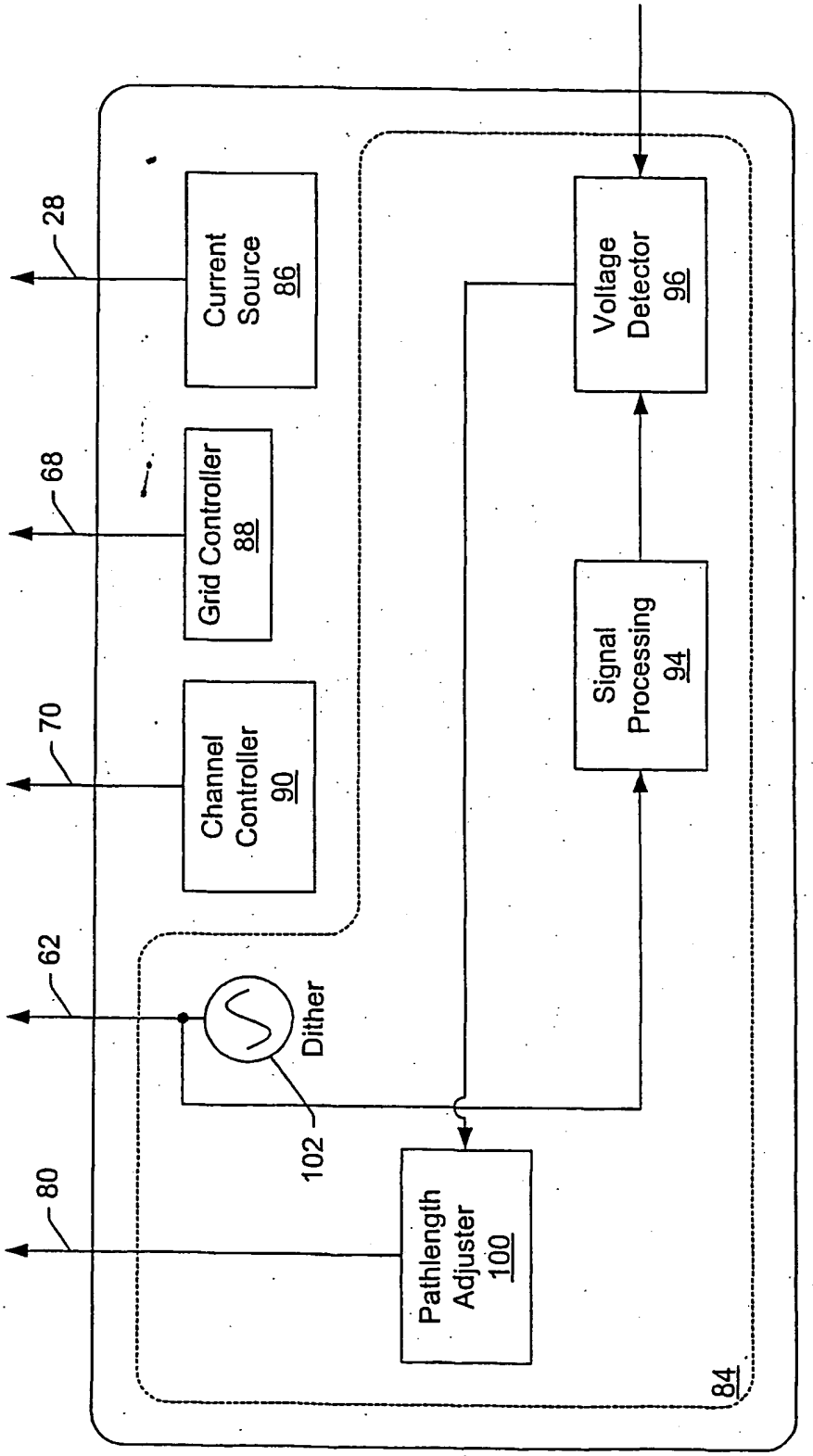

28
Current Source 86
68
Grid Controller 88
70
Channel Controller 90
62
Dither
102
80
Pathlength Adjuster 100
Voltage Detector 96
Signal Processing 94
84

Fig. 4

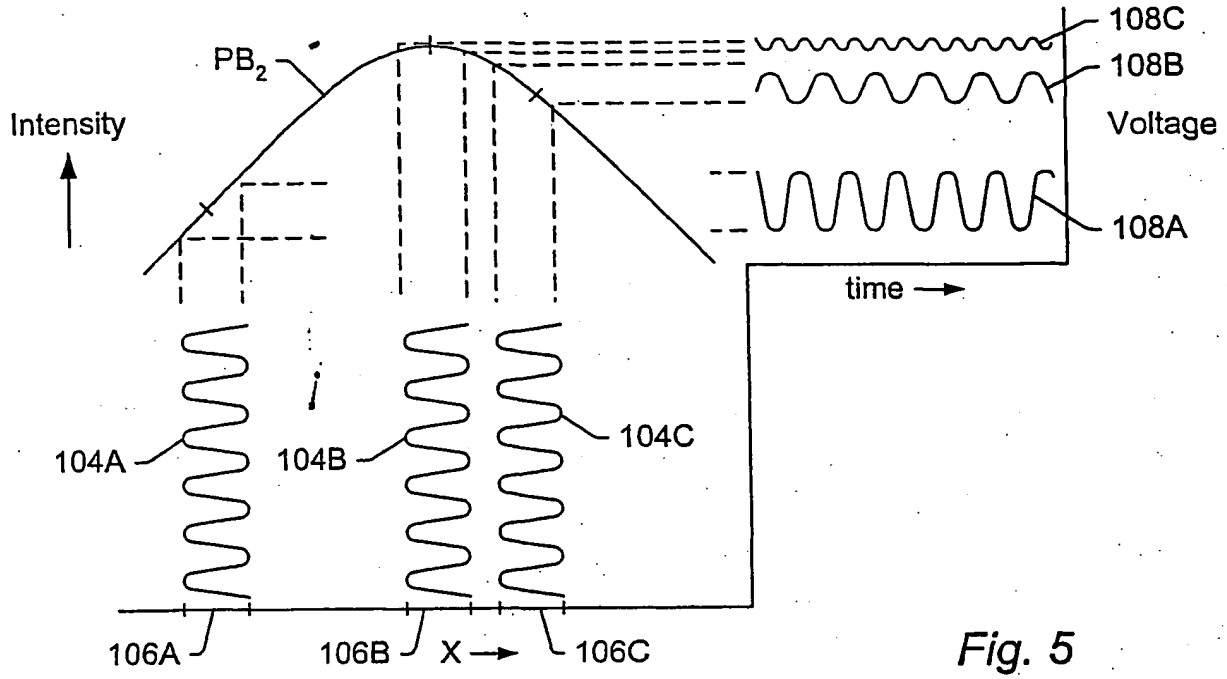
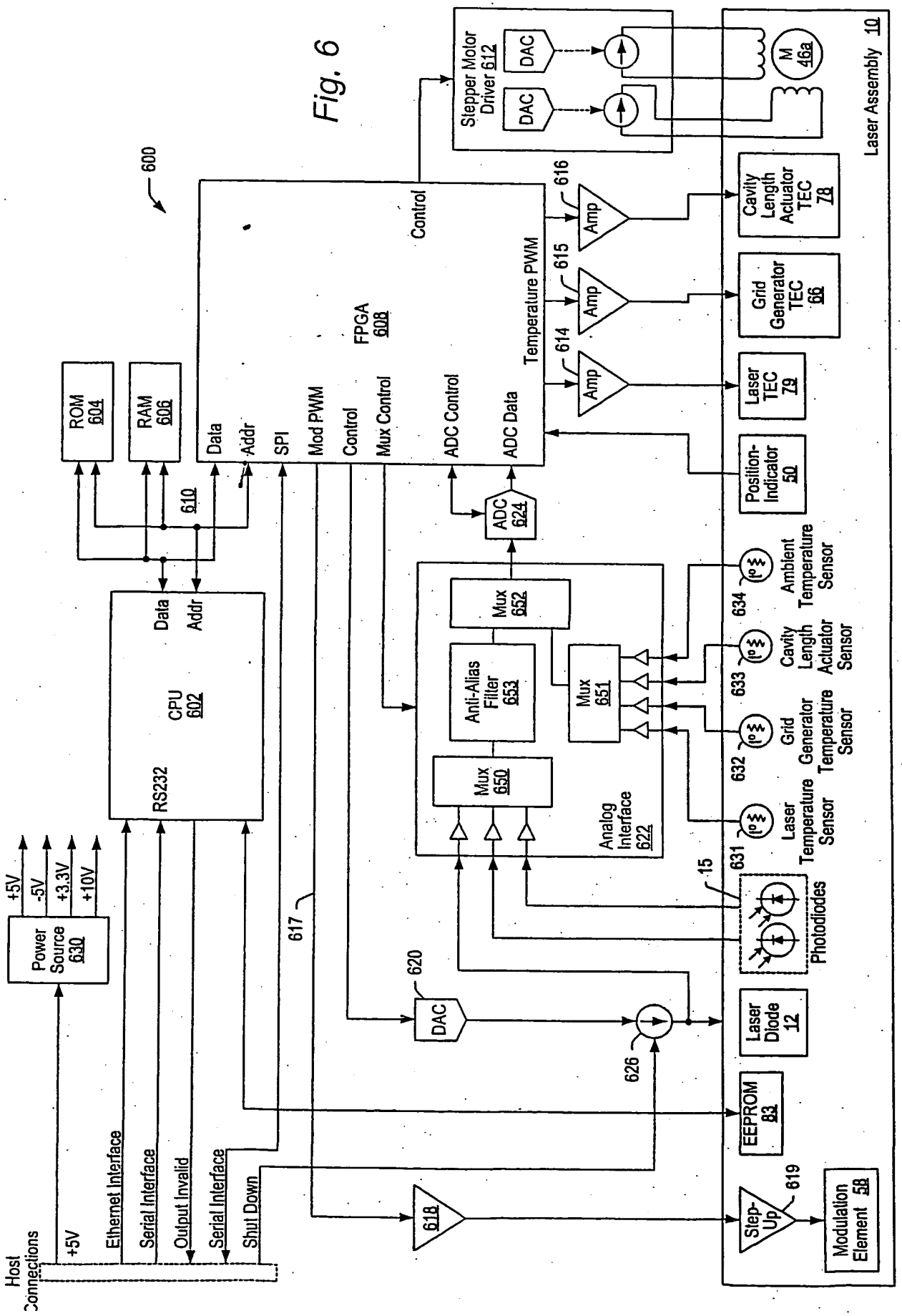

PB2
Intensity
108C
108B
Voltage
108A
time
104A
104B
104C
106A
106B
X
106C

Fig. 5

Fig. 6


600
Laser Assembly 10
Stepper Motor Driver 612
DAC
DAC
M 46a
Control
616
Amp
Cavity Length Actuator TEC 78
615
Amp
Grid Generator TEC 66
614
Amp
Laser TEC 79
Temperature PWM
FPGA 608
ROM 604
RAM 606
Data
Addr
SPI
Mod PWM
Control
Mux Control
ADC Control
ADC Data
610
Position-Indicator 50
ADC 624
Mux 652
Anti-Alias Filter 653
Mux 651
Mux 650
Analog Interface 622
Ambient Temperature Sensor
634
Cavity Length Actuator Sensor
633
Grid Generator Temperature Sensor
632
Laser Temperature Sensor
631
15
Photodiodes
Data
Addr
CPU 602
RS232
+5V
-5V
+3.3V
+10V
Power Source 630
617
620
DAC
626
Laser Diode 12
EEPROM 83
618
619
Step-Up
Modulation Element 58
Host Connections
+5V
Ethernet Interface
Serial Interface
Output Invalid
Serial Interface
Shut Down

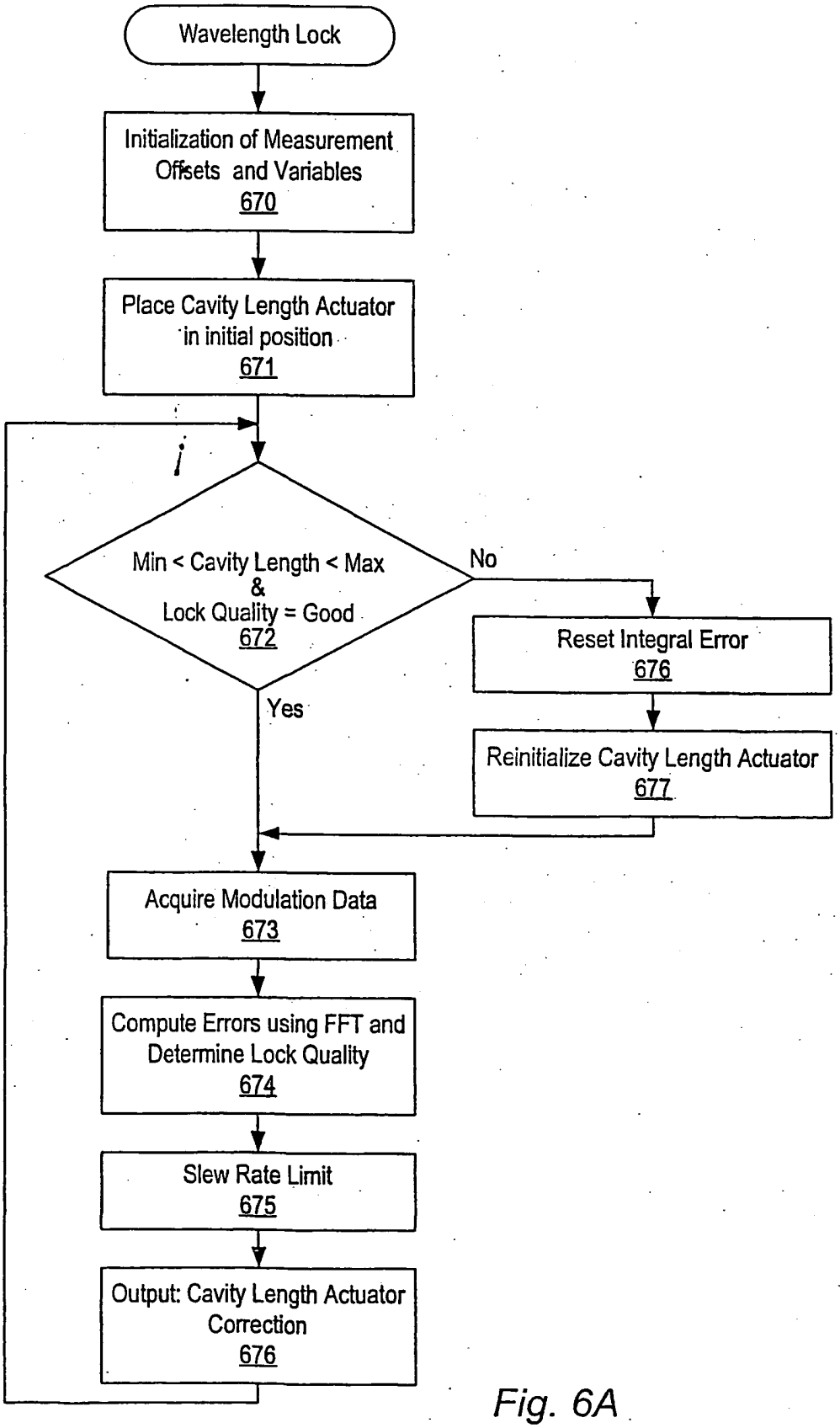

Wavelength Lock
Initialization of Measurement Offsets and Variables
670
Place Cavity Length Actuator in initial position
671
i
Min < Cavity Length < Max
&
Lock Quality = Good
672
No
Reset Integral Error
676
Reinitialize Cavity Length Actuator
677
Yes
Acquire Modulation Data
673
Compute Errors using FFT and Determine Lock Quality
674
Slew Rate Limit
675
Output: Cavity Length Actuator Correction
676

Fig. 6A

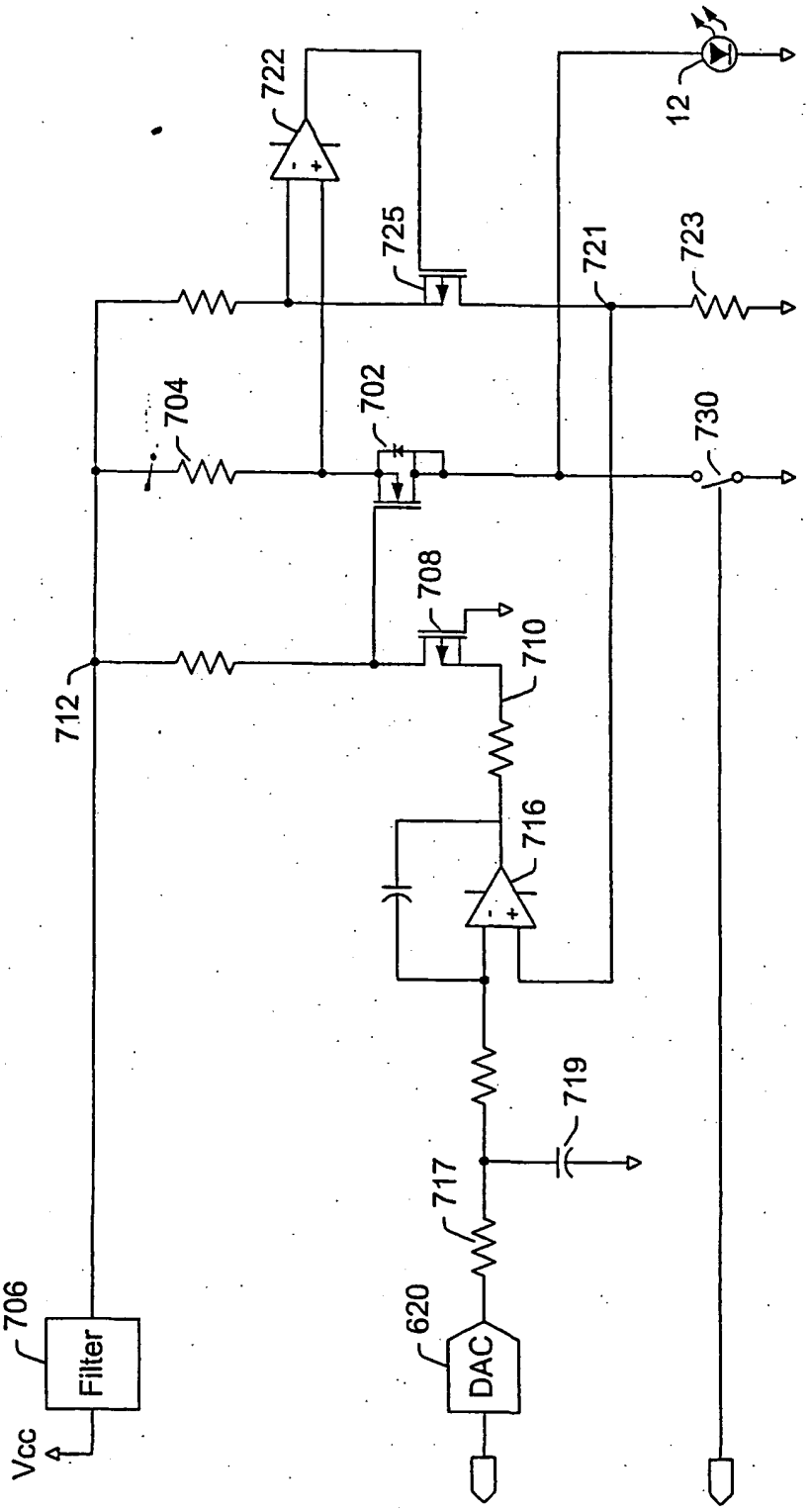

722
12
725
721
723
704
702
730
708
710
712
716
719
717
706
Filter
620
DAC
Vcc

Fig. 7

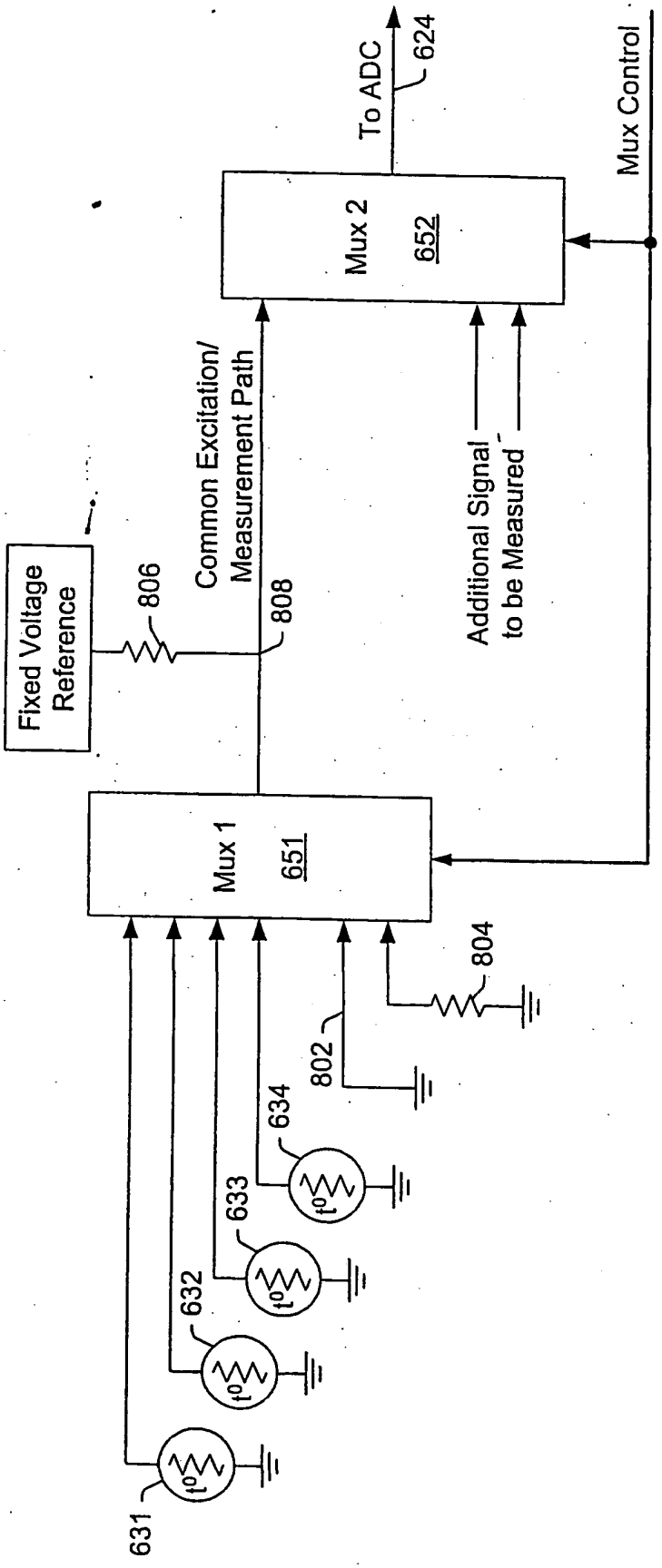

To ADC
624
Mux Control
Mux 2
652
Common Excitation/
Measurement Path
Additional Signal
to be Measured
Fixed Voltage
Reference
806
808
Mux 1
651
804
802
634
633
632
631

Fig. 8

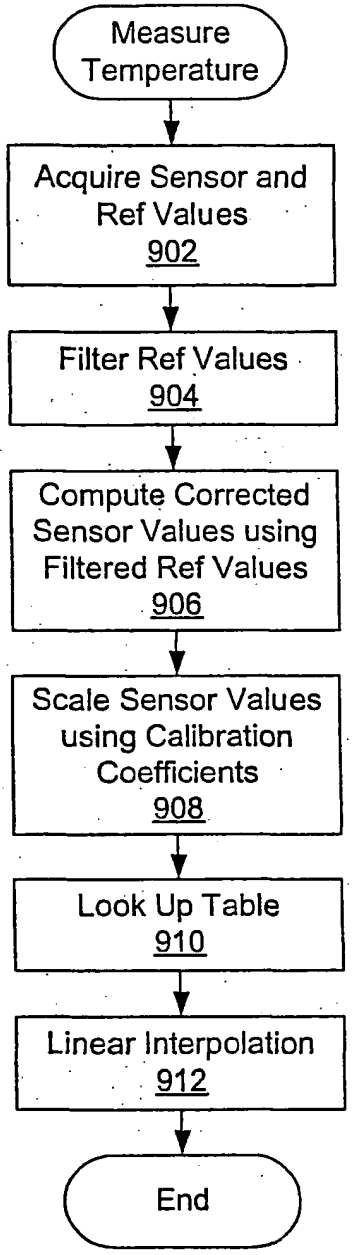

Measure Temperature
Acquire Sensor and Ref Values 902
Filter Ref Values 904
Compute Corrected Sensor Values using Filtered Ref Values 906
Scale Sensor Values using Calibration Coefficients 908
Look Up Table 910
Linear Interpolation 912
End

Fig. 9

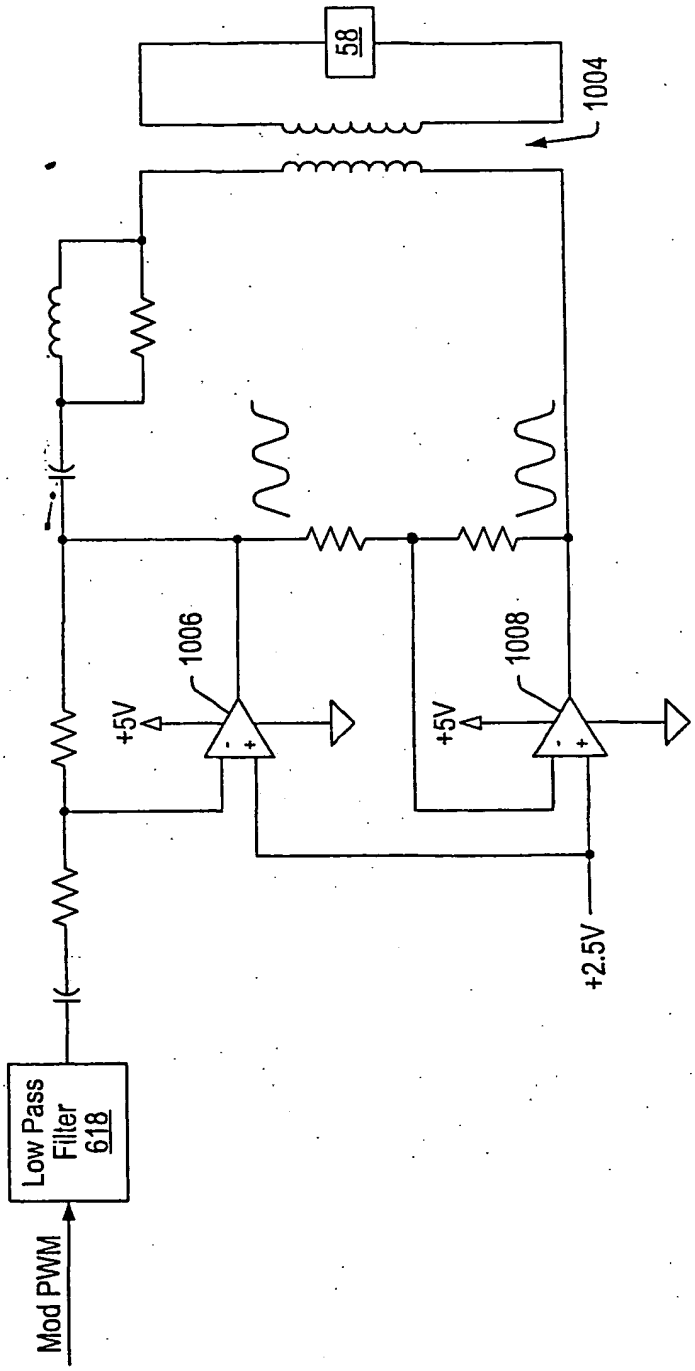


Fig. 10